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[S21 A HYPOTHETICAL 32-BIT PROCESSOR](#)

This is a typical simple 32-bit CPU. It has a three-address instruction architecture, with 32 registers and load/store instructions. This document presents only S21 assembly language view. It does not give details about microarchitecture (such as pipeline). S21 has three-address instruction set. A general format of an instruction (register to register operations) is: $op\ r1\ r2\ r3$ means $R[r1] = R[r2]\ op...$

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Control Unit Control Signal from Example RW Two approaches: Perform read/write operations from/to memory. MR Hardwired Enable the chip select of the memory. Microprogram LD Load data from data bus to MDR. Single cycle datapath requires: AD Load address from MAR to address bus. True stable \rightarrow hardwired solution. LA Multicycle datapath control may be defined through: Load the rightmost 4 bits of IR to MAR. WR Mi...

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[L?-LCD_27_OCT_2010_DRUCKVERSION_L?-LCD_2010.QXD](#)

STANDARD CHARACTER MODULES YMS 122-01 12 CHAR x 2 LINE, 1/16 DUTY, 1/5 BIAS EXTERNAL DIMENSION AND DISPLAY PATTERN MECHANICAL DATA ABSOLUTE MAXIMUM RATINGS ITEM SPECIFICATION UNIT
PARAMETER SYMBOL MIN. MAX. UNIT
Module Size (W x H x T) 55.7 x 32.0 x 9.8 mm
Supply Voltage Logic VDD - VSS -0.3 7.0 V
Viewing Area (W x H) 46.7 x 17.5 mm
Supply Voltage Drive VDD - VEE VDD -10 VDD +0.3 V
Character Size (...)





















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